IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF MASSACHUSETTS

SINGULAR COMPUTING LLC, Plaintiff, v. GOOGLE LLC, Defendant.	C.A. No. 1:19-cv-12551-FDS

GOOGLE LLC'S MEMORANDUM OF LAW
IN SUPPORT OF RULE 12(B)(6) MOTION TO DISMISS
FIRST AMENDED COMPLAINT FOR
LACK OF PATENTABLE SUBJECT MATTER

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I. INTRODUCTION

The patents in suit[1] claim a processor or other device for performing "low-precision, high-dynamic range" arithmetic. But Singular didn't invent low-precision arithmetic, which has existed in human endeavor for as long as there has been arithmetic and has existed in the field of computing since its advent. Nor did Singular invent high dynamic range, which is nothing more than a wide span of numbers. Nonetheless, the patents in suit attempt to monopolize the abstract idea that when doing math, sometimes close enough suffices. This idea is a part of daily life; for example, tipping to a round number at a restaurant rather than exactly 15% or 20%. Just claiming this idea in the computing realm, as Plaintiff did, is not patentable.

Performing calculations with a computer has always involved some imprecision. Computers represent numbers with a finite number of bits, yet some numbers require more bits, and some—the fraction 1/3 and the concept of *pi* being common examples—require an infinite number. So, when computers truncate numbers to meet their number format, some degree of imprecision arises relative to a calculation that would otherwise involve more digits than the computer's format accommodates.

Claiming this abstract idea on a low-precision, high dynamic range ("LPHDR") processor neither makes it less abstract nor adds an inventive concept. In a computer, a number is represented by a string of bits of a particular "width" (*e.g.*, 8-bit, 16-bit, 32-bit, or 64-bit). Because numbers are typically represented in a "floating point" format that follows a scientific notation format (*e.g.*, 1.25×10^{1}), the bits are used to express both precision (the left side, *i.e.*, 1.25) and range (the exponent on the right side). A floating-point format can provide more

[1] U.S. Patent Nos. 8,407,273; 9,218,156; and 10,416,961. *See* Dkt. 37, Amended Compl. ("FAC") ¶ 27. In this Memorandum, all references to the common specification refer to the '273 Patent.

precision by using more bits on the left side or provide more range by using more bits for the exponent. Thus, for a fixed processing bit-width (*i.e.*, 16-bit, 32-bit, and 64-bit), the greater the precision, the less the dynamic range (and vice versa). A LPHDR processor is nothing more than the application of the patent's abstract idea to the context of computing. By assigning more data bits to range than to precision, a LPHDR processor has less precision, but more dynamic range.

The patents in suit do not disclose a new (or indeed any) way to store numbers in a low-precision format or with a high dynamic range; instead, they rely on the skilled artisan's knowledge of conventional approaches to LPHDR representations. The purported inventive concept appears, at most, to be the recognition that in some computing applications, some level of imprecision may be acceptable. But the specification admits that prior implementations recognized that applications could accept various levels of imprecision, and that not every application required the same level of precision. The claims therefore offer no improvement of computing technology nor any inventive concept that would render them patentable.

Plaintiff responded to Google's prior motion to dismiss by amending the complaint to add supposed "Claimed Advance" allegations. Specifically, Plaintiff's first amended complaint ("FAC") identifies three purported "examples of invention." Two of these examples simply restate the abstract idea of doing low-precision arithmetic using known mathematical techniques and rely on the skilled artisan's knowledge of conventional approaches to LPHDR representations; therefore, they do not supply an inventive concept. The third example identifies a computer architecture having one hundred more LPHDR arithmetic units than non-LPHDR units. But the specification admits that this architecture was conventional and existed in prior implementations; therefore, it too cannot satisfy *Alice*, even at the motion to dismiss stage.

In sum, Plaintiff's FAC fails to overcome the simple fact that the claims are directed to an abstract idea, and Plaintiff is unable to plead any inventive concept to salvage them. Dismissal of Plaintiff's case is therefore appropriate.

II. BACKGROUND

The patents in suit are directed to a "processor or other device" that "includes processing elements designed to perform arithmetic operations." '273 Patent at Abstract. The "Summary" states that, in "some embodiments," "'low precision' processing elements perform arithmetic operations which produce results that frequently differ from exact results by at least 0.1% . . . ." *Id.* at 2:28-31. It goes on to assert that "[t]his is far worse precision than the widely used IEEE 754 single precision floating point standard." *Id.* at 2:31-33. Analyzing the asserted claims therefore requires some background on how computers handle arithmetic operations, including the use of floating-point numbers. This background can be gleaned from case law, the common specification of the patents in suit, and a standard that the common specification references.

A. Computing processors have long used floating-point number formats.

Processors have for decades performed arithmetic operations using a floating-point number format. Several courts, including the Federal Circuit, have explained this format:

> In floating point format, data is represented by the product of a fraction, or mantissa, and a number raised to an exponent. For example, a number *n* can be represented in base 10 by
>
> $$n = m \times 10^{e},$$
>
> where *m* is the mantissa and *e* is the exponent. If *m* equals 2 and *e* equals 1, *n* equals 20; if *m* equals 2 and e equals -1, then *n* equals 0.2. . . .

Silicon Graphics, Inc. v. ATI Techs., Inc., 607 F.3d 784, 787 (Fed. Cir. 2010); *see also Uniloc USA, Inc. v. Rackspace Hosting, Inc.*, 18 F. Supp. 3d 831, 834 (E.D. Tex. 2013). In a simple example of a number format, if an integer (whole number) format were used without any

exponent, then two digits would allow representing numbers from 1 to 99. By contrast, in the simplest example of the format described in *Silicon Graphics* with two digits in base 10, *i.e.*, m and e being allowed one digit each, the range of numbers represented would be from 1 (1×10^0) to 9 billion (9×10^9). Using this format affects precision: the number 9 or 10 can be expressed exactly (9×10^0 or 1×10^1), but unlike a two-digit integer format, there is no precise way to express the number 11, nor is there any precise way to express a number between 8 billion and 9 billion. In the computing context, floating-point representation widens the range of numbers that can be represented using a given number of bits (each of which is a binary digit), but using bits for the exponent reduces precision relative using those same bits for the mantissa.

B. The IEEE 754 standard describes a floating-point number's elements and the potential tradeoff between precision and dynamic range.

The IEEE Standard for Floating-Point Arithmetic (IEEE 754) was first issued in 1985 and is expressly referenced in the specification;[2] it established the standardized floating-point number format and provides background regarding conventional concepts that are relevant here.

Format: A binary floating-point number has a "numerical value, if any, [that] is [i] the signed product of its [mantissa][3] and [ii] two raised to the power of the exponent." IEEE 754 at 2. As the patent specification explains, floating-point numbers allow for a much wider dynamic range of calculations than integers (*i.e.*, 1, 2, 3, etc.) because a sequence of the same number of digits can represent a much wider range of numbers. '273 Patent at 5:25-30. That is, a floating-point number, like scientific notation, has an exponent that establishes the range of numbers the

[2] '273 Patent at 2:32-33. Google is filing a concurrent motion for judicial notice for the 1985 version of the IEEE 754 referenced in the specification of the patents in suit. While judicial notice of IEEE 754 is appropriate for the reasons set forth in the concurrent motion, it is used herein only to provide background information.

[3] IEEE 754 uses the term "significand" to refer to what the case law and other sources call the "mantissa." For simplicity, this Memorandum consistently uses the term "mantissa."

floating-point format can represent. IEEE 754 at 2. But that additional range comes at some loss of precision: floating-point representations have to be rounded to fit within the number of digits available for the mantissa. *Id.* at 5. By contrast, real numbers can have many or even an infinite number of digits in the mantissa: two examples are (i) the fraction ⅓, which is 0.33 repeating infinitely when represented as a decimal, and (ii) the concept of *pi*, which continues infinitely.

Precision. All floating-point number formats must have a specified precision level, which is nothing more than the number of digits in the mantissa. *Id.* at 2 (defining "significand"). As with the digits available for paper-and-pencil scientific notation, the bits available for the floating-point number representation are allocated to the mantissa, the exponent, or some other component (*e.g.*, a sign bit or "not a number" indicator). As reflected in Table 1, the IEEE standard had four different precision levels depending on the number of available bits. *Id.* at 3 & Table 1. As Table 1 depicts, the standard also includes "extended" formats, which can have a variable number of bits in the mantissa (a.k.a. "significand" or "p" in Table 1) and a wider (and also variable) exponent range, relative to the corresponding "basic" format. *See id.* at Table 1.

C. The common patent specification admits conventional computing implementations (i) had high dynamic range; (ii) used low precision; and (iii) included multiple arithmetic units.

The patent specification refers to then-existing, conventional computing implementations that used low-precision high dynamic range number formats in conventional computing implementations. It starts by explaining that prior art "array processors" had been built with varying bit-widths; precision would vary with bit-width. '273 Patent at 3:57-60, 3:65-4:6. The specification also explains, as Plaintiff alleges in its FAC, that "[t]he 'dynamic range' of the inputs to the execution unit . . . is the range in value of inputs that can be operated upon by that unit." FAC ¶ 34; *see* '273 Patent at 2:35-39. It then gives a specific example of low-precision, high dynamic range GPUs that "include support for 16 bit floating point values." '273 Patent at

5:11-17. Quoting a "late 2008" Wikipedia entry, the specification states that such formats have the advantage of a higher dynamic range than fixed point integers while also saving space compared to a 32-bit floating point format at the cost of reduced precision. *Id.* at 5:26-38.

The specification also describes conventional processors with multiple arithmetic units. It explains that existing GPUs—which had both (a) arithmetic units at various bit widths and (b) a precision level that Plaintiff alleges is low (*e.g.*, 16-bit)—used a "computing model . . . sometimes based on having thousands of nearly identical threads of computing . . . which are executed by a collection of SIMD-like internal computing engines . . . ." *Id.* at 5:1-4.[4] Significantly, the specification explains that one variety of SIMD processors, "array processors," use an entire "grid" of "processing elements" that perform arithmetic based on instructions "broadcast to the PEs from a central control unit." *Id.* at 3:43-44, 3:49-51, 3:57-58, & Fig. 2.

III. PLAINTIFF'S ALLEGED REPRESENTATIVE CLAIMS

The FAC alleges infringement of several claims from each of the patents in suit, but it also alleges that three of those claims are "representative" in its description of the patents' purported "claimed advance"—claim 53 of the '273 Patent, claim 7 of the '156 Patent, and claim 4 of the '961 Patent. FAC ¶¶ 31, 47, 64. Thus, the remainder of this Memorandum focuses on those three representative claims.[5]

[4] SIMD was a conventional kind of computer that stands for "single instruction multiple data" and refers to a kind of processor that "follow[s] a sequential program, with each instruction performing operations on a collection of data." '273 Patent at 3:40-41. A SIMD computer has many processing elements that perform the *same* instruction (e.g., an arithmetic operation) on *different* data inputs; the instruction is broadcast from a "central control unit" and then being performed by processing elements on its "local data." *Id.* at 3:49-54.

[5] Courts may decide patentability based on representative claims. *See, e.g., Two-Way Media Ltd. v. Comcast Cable Commc'ns, LLC*, 874 F.3d 1329, 1333 (Fed. Cir. 2017); *Content Extraction & Transmission LLC v. Wells Fargo Bank, N.A.*, 776 F.3d 1343, 1348 (Fed. Cir. 2014).

Claim 53 of the '273 Patent includes elements common to all claims allegedly infringed: (a) "[a] device comprising at least one first low precision high dynamic range (LPHDR) execution unit"; (b) "a first operation" (performed on the first input signal); (c) "a first input signal representing a first numerical value"; (d) "a first output signal representing a second numerical value"; (e) a "dynamic range of possible valid inputs to the first operation . . . at least as wide as from 1/1,000,000 through 1,000,000"; (f) "for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input"; and (g) "the number of LPHDR execution units in the device exceeds" by at least 100 the number of "execution units in the device adapted to execute" the operation of multiplication "on floating point numbers that are at least 32 bits wide."

Elements a-d claim a low-precision, high dynamic range unit to execute computing operations, an input to that unit, an operation on that input, and an output of that operation, where both the input and the output represent numerical values. FAC ¶ 32.

Element e claims the minimum dynamic range of 1/1,000,000 to 1,000,000, which is the span of "possible valid inputs" to the first operation.

Element f claims an imprecision level for the LPHDR execution unit. While the language regarding this element is arguably ambiguous, for purposes of this Motion, Google adopts the understanding that Plaintiff set forth in its FAC. This element first specifies a minimum percentage of available inputs from the dynamic range (the "possible valid inputs") on which the operation has to be performed when determining the execution unit's imprecision level. FAC

¶¶ 36, 52, 69. That is the "X=5%" component. Second, it specifies the minimum amount by which the output of doing the first operation on the first input signal using the execution unit has to differ from the result of doing an operation as an "exact mathematical calculation" on the "numerical value" that an input signal represents; rather than looking at a single instance of this difference, the claim looks at the average difference from the "repeated" performance of the operation. FAC ¶¶ 35-36, 51-52, 68-69. This difference is the "Y=.05%" component.[6]

Element g requires that the "device" have 100 more LPHDR execution units than it has execution units that perform multiplication on 32-bit floating-point numbers.[7]

IV. LEGAL STANDARD

The Supreme Court first addressed whether claims directed to computing articles or methods that performed mathematical operations are patentable in the 1970s. In *Parker v. Flook*, the Court held that "'if a claim is directed essentially to a method of calculating, using a mathematical formula, even if the solution is for a specific purpose, the claimed method is nonstatutory [subject matter under § 101].'" 437 U.S. 584, 595 (1978) (quoting *In re Richman*, 563 F.2d 1026, 1030 (C.C.P.A. 1977)). Prior to that, in *Gottschalk v. Benson*, the Court held that an algorithm for converting "binary coded decimal" (BCD) numbers to "pure" binary numbers

[6] Claim 7 of the '156 Patent incorporates the same error-related percentages as claim 53 of the '273 Patent; and in claim 4 of the '961 patent, X=10% and Y=0.2%. '273 Patent at 32:3, 32:11; '156 Patent at 29:62, 30:2; '961 Patent at 30:63, 31:2.

[7] The other two representative claims share this same core structure. Representative claim 7 of the '156 Patent, however, includes two additional elements: "at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit" and "a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FGPA), a microcode-based processor, a hardware sequencer, and a state machine." '156 Patent at 30:5-17. Of these two additional elements, representative claim 4 of the '961 Patent includes the first element—"at least one first computing device adapted to control . . . ," but not the second element—"a central processing unit (CPU) . . . ." '961 Patent at 30:17-51. Claim 4 of the '961 Patent also does not require at least 100 more LPHDR execution units than 32-bit multiplication units.

lacked patentability because "in practical effect" allowing that patent would have meant allowing a "patent [on] an idea." 409 U.S. 63, 71-72 (1972).

More recently, the Court developed a two-stage framework to assess whether a claim falls outside Section 101. *Alice Corp. v. CLS Bank Int'l*, 573 U.S. 208, 217-18 (2014). Under the *Alice* framework, a claim is not patentable where (1) it is directed to a patent-ineligible concept, *i.e.*, a law of nature, natural phenomenon, or abstract idea, and (2) the particular elements of the claim, considered both individually and as an ordered combination, lack an inventive concept sufficient to transform the nature of the claim into a patent eligible application. *Id.*; *Elec. Power Grp. LLC v. Alstom SA*, 830 F.3d 1350, 1353 (Fed. Cir. 2016). The Federal Circuit has "described the first-stage inquiry as looking at the 'focus' of the claims, their 'character as a whole,' and the second-stage inquiry (where reached) as looking more precisely at what the claim elements add." *Elec. Power Grp.*, 830 F.3d at 1353. Furthermore, as part of the overall patentability analysis, the Federal Circuit has distinguished between non-patentable "uses of existing computers as tools in aid of processes focused on 'abstract ideas'" and patentable "computer-functionality improvements." *Id.* at 1354 (distinguishing *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327 (Fed. Cir. 2016)).

Although the courts must accept *plausible* factual allegations as true when deciding patentability at the Rule 12(b)(6) stage, *Aatrix Software, Inc. v. Green Shades Software, Inc.*, 882 F.3d 1121, 1125 (Fed. Cir. 2018), conclusory allegations—including conclusory assertions of an inventive concept—are insufficient to survive an otherwise proper motion to dismiss for lack of patentability. *See, e.g.*, *RingCentral, Inc. v. Dialpad, Inc.*, 372 F. Supp. 3d 988, 995 (N.D. Cal. 2019); *Rothschild Dig. Confirmation, LLC v. Skedulo Holdings, Inc.*, No. 3:19-cv-02659-JD, 2020 WL 1307016, at *2 (N.D. Cal. Mar. 19, 2020).

V. ARGUMENT

Under *Alice*'s two-part rubric, the asserted claims are, at the first step, directed to an abstract idea: using a LPHDR execution unit to execute an operation on a signal representing a first numerical value to produce a second numerical value that is intended to be less precise. The notion of doing less precise calculations is part of human history, including the ancient Greeks calculating a square root through iterative approximation[8] and a modern-day diner trying to approximate out a 20% tip quickly in a restaurant. The patents in suit rest on the same idea: don't waste time or resources on needless precision when close enough will suffice. Doing such low-precision calculations on numbers that have a high dynamic range is equally abstract because a high dynamic range is just a span of values that a numerical representation can encompass. To take an example from long-extant principles outside computing, a single-digit representation using the Arabic numeral system can represent 9 different values, which is not an especially high dynamic range. By contrast, a two-digit representation for base 10 scientific notation can represent, as set forth above, values ranging from 1 to 9 billion. High dynamic range is, literally, just mathematics, and it is completely abstract, irrespective of whether it is used for low-precision calculations or higher-precision calculations.

At step 2 of the *Alice* inquiry, there is no inventive concept; Plaintiff has not pleaded, nor do the patents in suit claim, any novel technological improvement. Plaintiff's FAC identifies three purported "inventions": the first two involve using well-known mathematical techniques—logarithmic number system and floating-point arithmetic—with particular bit-widths for the mantissa and exponent. But these purported inventions are not claimed, and thus they are not relevant to the *Alice* analysis; furthermore, they are themselves just abstract ideas that are also

[8] *See, e.g.*, Michael Lahanas, *Heron's Mathematics*, http://www.hellenicaworld.com/Greece/Science/en/HeronsMath.html (retrieved April 16, 2020).

entirely conventional. The third purported "invention" just applies LPHDR processing, with specific mantissa and exponent bit-widths, on conventional computer processors that had multiple arithmetic units. The representative claims of the '273 and '156 Patents also claim at least 100 more low-precision execution units than higher-precision execution units, if any; however, the specification associates nothing inventive or beneficial with this arbitrary number. Given the absence of any identified benefit or technical problem solved by that threshold, whether in the specification or the FAC, it does not reflect any technological improvement. Thus, the representative claims cannot meet *Alice* step 2's inventive concept requirement.

The asserted claims are abstract under the fundamental and still-operative principles set forth in *Gottschalk* and *Flook* in the 1970s. The claims do nothing more than take concepts that are inherent in numeric representations—precision and range—and purport to apply them on a computer processor. This is no less abstract than using a computer to convert from binary-coded decimals to "true" binary as in *Gottschalk* or to run a known algorithm for calculating alarm limits for an industrial process as in *Flook.*

A. The asserted claims are directed to the abstract idea of doing an arithmetic calculation with an intended degree of imprecision.

The focus of the representative claims and their character as a whole confirm that they are abstract at *Alice* step one. Specifically, the representative claims are directed to the abstract idea of using (a) a "low precision high dynamic range (LPHDR) execution unit" to (b) "execute a first operation on a first input signal representing a first numerical value" to (c) "produce" a "second numerical value." Each part of this abstract idea is explained in further detail below.

The term "low precision" means that the execution unit is not adapted to calculate the precisely correct mathematical result every time it performs an arithmetic operation, but instead has an anticipated range of imprecision. Allowing for imprecision can, according to the

specification, result in more efficient use of processing resources, while the level of imprecision can be adapted to a level acceptable to whatever application that calculation is being applied. '273 Patent at 7:27-39. This is the same (abstract) idea as calculating a 20% tip on a dinner check of $24.76 as $5 rather than trying to calculate the exact value of 20% of that dinner check: you know that $5 is 20% of $25 and thus a much easier number to calculate than the exact value, from which it will differ by less than 20 cents, *i.e.*, 20% of $1. Most diners are willing to pay a few cents over 20% in order to save the time and effort of exactly calculating the tip. Intended imprecision was, according to the specification itself, also used in computing, including prior art GPUs that included support for 16-bit floating-point representations. *E.g.*, '273 Patent at 5:16-30.

Executing a low-precision calculation in a unit that has "high dynamic range" means only that the execution unit can represent a relatively broad range of numbers. This includes small numbers such as 1/65,000 as well as large numbers such as 65,000. '273 Patent at 29:65-30:16. Wide dynamic ranges have long existed outside computing. In the instance of tipping described above, a diner may use approximate numbers to calculate the tip more easily whether it's a $9.76 check at a diner for one person, $24.76 for multiple people, or $148.57 at a gourmet restaurant. In the realm of mathematics specifically, any person using scientific notation knows that the more digits one uses for the exponent, the larger the range of values that the notation format can cover. In fact, any numeric representation, if it has a limited number of digits, will have a range of values it covers. The patent specification itself recognizes this abstract idea as present in pre-existing implementations, noting that a floating-point representation offers wider dynamic range than integers. '273 Patent at 5:25-30.

The claimed low-precision and high-dynamic range execution unit is entirely conventional and does not constitute an improvement to computing technology under either *Enfish* or *DDR Holdings v. Hotels.com, LP*, 773 F.3d 1245, 1259 (Fed. Cir. 2014). Indeed, the

specification itself identifies processor implementations that intentionally used low precision and also had high dynamic range. '273 Patent at 5:11-30; *see infra* Part V.B.

To the extent there is any suggestion of an invention in the specification, it appears, at most, to be the realization that LPHDR processing may be useful in certain applications. '273 Patent at 7:5-11. But that "realization" is not reflected in the claims, which attempt only to claim a mathematical *result* rather than any allegedly inventive application of the abstract idea. *See Internet Patents Corp. v. Active Network, Inc.*, 790 F.3d 1343, 1348 (Fed. Cir. 2015). The same is true of the FAC's allegations regarding "advantages": those allegations just express the conventional, well-known idea that using LPHDR would use fewer resources while allowing for a wider dynamic range, relative to higher precision or lower-dynamic range representations. *Compare* FAC ¶¶ 44a-c, 61a-d, 75a-d (noting speed, efficiency, and dynamic range of LPHDR processing), *with* '273 Patent at 5:26-30 (in GPUs, 16-bit floating point's advantage "over 8-bit or 16-bit binary integers is that the increased dynamic range allows for more detail to be preserved" while "[t]he advantage over 32-bit single precision binary formats is that it requires half the storage and bandwidth"). As with the claims that the Federal Circuit found non-patentable in *Internet Patents*, the representative claims "contain[] no restriction on how the result is accomplished." 790 F.3d at 1348. Similarly, in *Electric Power Group*, the Federal Circuit explained that there exists "an important common-sense distinction between ends sought and particular means of achieving them, between desired results (functions) and particular ways of achieving (performing) them." 830 F.3d at 1356. The same principle applies here: the representative claims are directed to abstract ideas under *Alice* step 1.

B. The purported "examples of invention" Plaintiff identifies are not inventive concepts that make the representative claims patentable at *Alice* step 2.

Under *Alice* step two, the question is whether a claim nonetheless "contains an inventive concept sufficient to transform the claimed abstract idea into a patent-eligible application." 573 U.S. at 221 (citations omitted). The focus at this step is on the individual elements or the ordered combination *apart from the abstract idea. Chamberlain Grp., Inc. v. Tectronic Indus., Co.*, 935 F.3d 1341, 1349 (Fed. Cir. 2019). Thus, "a claimed invention's use of the ineligible concept to which it is directed cannot supply the inventive concept that renders the invention 'significantly more' than that ineligible concept.'" *BSG Tech LLC v. BuySeasons, Inc.*, 899 F.3d 1281, 1290 (Fed. Cir. 2018).

Here, the FAC alleges several purported "examples of invention," but none provides an inventive concept that could establish patentability. Rather, the purported inventions simply describe performing the abstract idea using conventional computer processors, which is *a fortiori* insufficient to satisfy the inventive concept requirement of patentability. *Id*. Each of Plaintiff's three "examples of invention" is addressed below.

1. Logarithmic number system arithmetic at a particular bit width is abstract and conventional and not even claimed.

For representative claim 53 of the '273 Patent, Plaintiff asserts that it was inventive to use "a logarithmic number system format with an integer field of 5 bits plus a sign bit" where "[e]ach LPHDR unit is structured to transmit as outputs electrical signals that represent numbers using a logarithmic number system format with a fraction field of 6 bits plus a sign bit." FAC ¶ 39. Plaintiff makes the same assertion for the other two representative claims, except that the number of output bits varies. FAC ¶¶ 56, 71. But as the specification explains: "a Logarithmic Number System (LNS)" was "*well-understood by those having ordinary skill in the art.*" '273 Patent at 11:56-58 (emphasis added).

LNS arithmetic does not supply an inventive concept for several reasons. First, LNS arithmetic is no less abstract than LPHDR arithmetic generally. Slide rules have used a logarithmic number system to do arithmetic since the 17th century. HARRY HENDERSON, ENCYCLOPEDIA OF COMPUTER SCIENCE AND TECHNOLOGY 13 (2009) (Ex. 1). "[T]he slide rule's movable parts are marked in logarithmic proportions, allowing for quick multiplication, division, [and] the extraction of square roots." *Id.* The MIT Museum observed of the logarithm-scale slide rule that, "[f]rom the mid-19th century through the 1970s, every significant human-built structure has involved its use."[9] Even prior to *Alice*, the use of LNS arithmetic, had Plaintiff actually claimed it, would not have been patentable because it is "directed essentially to a method of calculating, using a mathematical formula." *Flook*, 437 U.S. at 595.

Second, as the specification admits, LNS arithmetic was "well-understood" in the art. Having conceded in the specification that LNS arithmetic was not novel, Plaintiff cannot now claim it as an inventive concept. Even at the Rule 12(b)(6) stage, a conclusory allegation of novelty is insufficient to avoid dismissal where the patentee points only to "well-understood, routine, conventional activity previously engaged in by researchers in the field." *Rothschild Dig.*, 2020 WL 1307016, at *5 (*citing Chamberlain*, 935 F.3d at 1349). Furthermore, as the district court explained in *RingCentral*, courts look to the language in the "claims or specification" that support the assertion that the identified problem is novel or that the claimed arrangement of elements yields any specific technical improvements over the prior art. 372 F. Supp. at 998. Not only does the FAC fail to identify any language in the specification that would meet this criteria, but the specification actually undercuts any claim of novelty as to LNS arithmetic because it (correctly) identifies the concept as well-understood in the art, as quoted above.

[9] https://mitmuseum.mit.edu/object-collection/slide-rules (retrieved April 16, 2020).

Third, although LNS arithmetic is insufficient to establish patentability in any event, Plaintiff cannot rely on it to establish patentability here because it *is not even claimed*. *Alice*, 573 U.S. at 221 ("[W]e must examine the elements of the claim to determine whether it contains an 'inventive concept.'"); *see also Synopsys, Inc. v. Mentor Graphics Corp*., 839 F.3d 1138, 1149 (Fed. Cir. 2016) (same); *Am. Axle & Mfg. Co. v. Neapco Holdings LLC*, 939 F.3d 1355, 1363 (Fed. Cir. 2019) (same).

2. Floating point number system arithmetic at a particular bit width is abstract and conventional and not even claimed.

For representative claim 53 of the '273 Patent, Plaintiff asserts two separate "inventions" based on using a "floating point number system": (1) using a floating point number system "with an exponent field of 5 bits plus a sign bit" and "a mantissa field of 10 bits plus a sign bit," FAC ¶ 40, and (2) using a floating point number system "with an exponent field of 7 bits plus a sign bit" and "a mantissa field of 7 bits plus a sign bit," FAC ¶ 41. Plaintiff makes the same allegations for representative claim 7 of the '156 Patent. FAC ¶¶ 57, 58. For representative claim 4 of the '961 Patent, Plaintiff makes only the 7 bit + 7 bit allegation. FAC ¶ 72. These allegations do not identify an inventive concept.

Identifying a specific number of bits in the exponent and/or the mantissa just restates the abstract idea of low-precision high dynamic range processing; that is, that more exponent bits provides greater dynamic range and fewer mantissa bits provides less precision. This does not suffice to supply an inventive concept. *Cf. Chamberlain*, 935 F.3d at 1349 (inventive concept or ordered combination must go beyond the abstract idea itself); *BSG Tech LLC*, 899 F.3d at 1290 (same). "[T]he focus of the claims" in this instance "is not on such an improvement in computers as tools, but on certain independently abstract ideas"—use of low-precision, high-dynamic range arithmetic—"that use computers as tools." *Elec. Power Grp.*, 830 F.3d at 1354.

Nor can Plaintiff argue that the particular bit widths specified, *i.e.*, 5 + 10 or 7 + 7, supply an inventive concept because they do not appear in the claims. *Alice*, 573 U.S. at 221. The FAC also offers no explanation for why the identified combinations of mantissa and exponent bits are anything other than arbitrary; it does not, for example, allege that the patentees discovered a usefulness of these particular combinations for a specific application. *Cf. Flook*, 437 U.S. at 594-95 (identification of alarm limits not patentable where inventors didn't identify any new discovery about the usefulness of a particular limit). To the contrary, the patent specification states that the appropriate precision (mantissa bits) and dynamic range (exponent bits) will vary by application. '273 Patent at 27:5-7 ("Besides having various possible degrees of precision, implementations may vary in the dynamic range of the space of values they process.").

In any event, the specification also explains that varying the number of bits used for mantissa and exponent was entirely conventional in computing at the time of the patent application. As the patent specification acknowledges in the discussion of GPUs referenced in Part II.C. *supra*, then-existing implementations used 16-bit floating-point representations when the application in question did not require a higher-precision 32-bit or 64-bit representation. '273 Patent at 5:11-30. Outside the field of computing, scientific notation embodies the idea that using more digits for an exponent widens the range of values that a particular notation form can cover, whereas using more digits for the mantissa will increase precision.

In summary, based on the pleadings alone, it is clear that having lower precision (via less bits in the mantissa) and/or higher range (via more bits in the exponent) was both abstract and conventional. Without offering some further pleading of an inventive step, Plaintiff's allegation is conclusory and insufficient to satisfy *Alice* step 2. *See RingCentral*, 372 F. Supp. 3d at 995; *Rothschild Digital*, 2020 WL 1307016, at *2.

3. The purported processor architecture features that Plaintiff identifies just re-state techniques that the specification admits are conventional.

For representative claim 53 of the '273 Patent and claim 7 of the '153 Patent, Plaintiff's "invention" allegations also say that the "example computer" includes "a far smaller number of execution units that each execute the operation of multiplication on floating point values that are at least 32 bits wide, that 'far smaller' number being at least 100 fewer than the number of LPHDR units in the computer." FAC ¶ 40, 56. For representative claim 7 of the '153 Patent and claim 4 of the '961 Patent, Plaintiff's "invention" allegations further state that the example computer includes (1) "a computing device that is any of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine, and that controls the operation of the LPHDR units" and (2) a "computing unit" that is "adapted to control the operation of the at least one first LPHDR execution unit." FAC ¶ 58, 62.

As to the at least 100 more LPHDR elements, the specification discloses that such computers existed in preexisting, conventional implementations; its discloses SIMD computers and computers with GPUs that included array processors with many arithmetic elements: "Array processors distribute data across a grid of processing elements (PEs). . . . Each PE performs the broadcast instruction on its local data . . . ." '273 Patent at 3:49-50, 3:52-53. The specification also admits that processing elements in a SIMD computer included a variety of bit-widths, "such as 1, 4, 8, and wider, and using floating point arithmetic." *Id.* at 3:58-60. It further explains that conventional implementations had applied the SIMD-like processing model into a "parallel processor . . . having thousands of nearly identical threads of computing . . . executed by a collection of SIMD-like internal computing engines," namely GPUs. *Id.* at 4:65-5:4. And the specification notesthat computers with conventional GPUs had both LPHDR and non-LPHDR

execution units. *See id.* at 3:6-18, 4:64-5:10; *see also id.* at 28:64-29:4. Having admitted in the specification that prior implementations included a very large number of processing elements, including LPHDR elements, the inclusion of at least 100 more LPHDR units than non-LPHDR units is entirely arbitrary. Indeed, the specification does not tie that threshold number of additional LPHDR units to any novel discovery, much less to any novel discovery beyond the "very large number" of LPHDR units already included in conventional prior art processors.

Likewise, the specification admits that the different kinds of processors that Plaintiff identifies as its "invention" in the FAC (*i.e.*, CPU, GPU, FGPA, microcode-based processor, hardware sequencer, state machine) all existed in the prior art. *Id.* at 3:30-39 (stating that these various types of processors existed at the time of the specification). The specification also confirms that SIMD computers, as an example, included a "central control unit" that controlled its low-precision processing elements by broadcasting a common instruction to them. 273 Patent, at 3:49-54; *see supra* Note 4. The patents in suit do not purport to improve on these conventional components.

The FAC's attempt to distinguish the representative claims over the conventional, prior art GPUs is inapposite. Plaintiff alleges that conventional GPUs did not have "execution units" with a "dynamic range at least as wide as from 1/1,000,000 through 1,000,000". *E.g.*, FAC ¶ 59. But, again, the recitation of a dynamic range for the representation of numbers is not inventive. Rather, a minimum range simply amounts to a minimum number of bits to use for the exponent of a computer's representation format. The idea that using additional exponent bits would expand dynamic range is explained in the 1985 IEEE standard, as well as integral to scientific notation and floating-point numbers; therefore, it does not aid patentability. *Compare* '273 Patent at 27:5-7 ("Besides having various possible degrees of precision, implementations may vary in the dynamic range of the space of values they process."), *with Flook*, 437 U.S. at 586 ("The patent

application does not purport to explain how to select the appropriate margin of safety, the weighting factor, or any of the other variables."); *see also Uniloc USA, Inc.*, 18 F. Supp. at 838 (finding claim that "merely constitutes an improvement on the known method for processing floating-point numbers" not patentable).[10]

The FAC further tries to distinguish conventional GPUs by arguing that they did not disclose transmitting "as an output for at least X = 5% of the possible valid inputs to that operation . . . numbers that differ by at least 0.05% from the result of an exact mathematical calculation of that operation on the numerical values of that same input." *E.g.*, FAC ¶ 59. But this part of the claim also fails to demonstrate an inventive concept because the 0.05% is entirely arbitrary and without any identified benefit. In fact, the specification disclaims the significance of any particular level of imprecision. '273 Patent at 27:58-62. Likewise, the specification disclaims the significance of the particular fraction of the results for which that mean error applies. *Id.* at 27:54-56, 27:60-62. This claim element does nothing more than instruct applying the abstract idea of an imprecise mathematical calculation, without offering "a particular concrete solution to a problem"; accordingly, it does nothing more than "attempt[] to patent the abstract idea of a solution to a problem in general." *Elec. Power Grp.*, 830 F.3d at 1356.

VI. CONCLUSION[11]

For the foregoing reasons, all the claims identified in Plaintiff's FAC as potentially infringed should be found unpatentable under Section 101, and this action should be dismissed.

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[10] In *Am. Axle & Mfg. Co. v. Neapco Holdings LLC,* the asserted claim was found *unpatentable* even where it included specific numerical parameters for application of a law of physics because it was merely directed to applying the law rather than to any improvements in the machine. 309 F. Supp. 3d 218, 225 (D. Del. 2018), *aff'd* 939 F.3d 1355 (Fed. Cir. 2019).

[11] Plaintiff does not allege any ordered combination of elements beyond what is discussed above in addressing the allegations in the "Claimed Advances" section of the FAC. Thus, the possibility of an ordered combination does not establish patentability. *See Maxon, LLC v. Funai Corp., Inc.*, 255 F. Supp. 3d 711, 720 (N.D. Ill. 2017), *aff'd* 726 Fed. App'x 797 (2018).

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Respectfully submitted,

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